REMARKS

Reconsideration of the above-identified application is requested in view of the remarks that follow.

In the August 12, 2004, Office Action in this application, the Examiner rejected claim 1 under 35 U.S.C. 102(b) as being anticipated by either the Talbot et al. '249 patent or the Lo et al. '750. As indicated above, claim 1 has been cancelled. New claim 2 has been added. For the reasons set forth below, Applicant believes that new claim 2 patentably distinguishes over the teachings of Talbot et al. '249 patent and the Lo et al. '750 patent, whether considered individually or in combination.

Both the Talbot et al. patent and the Lo et al. patent are directed to identification of problem areas on an integrated circuit die utilizing well known voltage contrast techniques. Given the resolution of today's die inspection systems, unless specific areas of interest are predefined for the die structure, these voltage contrast techniques can be both time consuming and labor intensive when applied to the entire die.

The claim 2 method utilizes voltage contrast characteristics, e.g. from a scanning electron microscope (SEM) image, for scanning individual integrated circuit cells. The method can be implemented in software using image pattern recognition for speedy fault identification.

Conventional voltage contrast comparison techniques are typically applied at the lower level process layer of the die structure, e.g. the metal1 (M1) – metal3 (M3) process layers, and the associated vias and contacts. Examples of these voltage contrast images are provided in Figs. 3C, 3D and 3F of the application. The bright/dark patterns of these images are fixed with respect to a normal standard cell. That is, the relative bright/dark contrast patterns among the same types of standard cells will be identical. In addition, the numbers of these bright contrast regions and dark contrast regions at a given site and a given topography will be the same for the same type of standard cell since the electrical paths from these contrast sites are identical. As a result, and as recited in claim 2, the contrast distributions of a selected standard cell can be used to differentiate problem cells from "good" cells. The physical location of the cells within a given integrated circuit structure can be extracted from the circuit's layout database.

Thus, failure analysis of integrated circuit structures in accordance with the claim 2 invention involves localizing the fault region under test to a smaller area of the circuit die. As is well known, with in localized area, replication of standard cells is very common. Cross-checking the voltage contrast characteristics of the device under test against the fault characteristics information in a cell reference library in accordance with the claim 2 method provides a fast and accurate technique for isolating problem areas in the die structure.

For the reasons set forth above, Applicant believes that the method recited in new claim 2 patentably distinguishes over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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